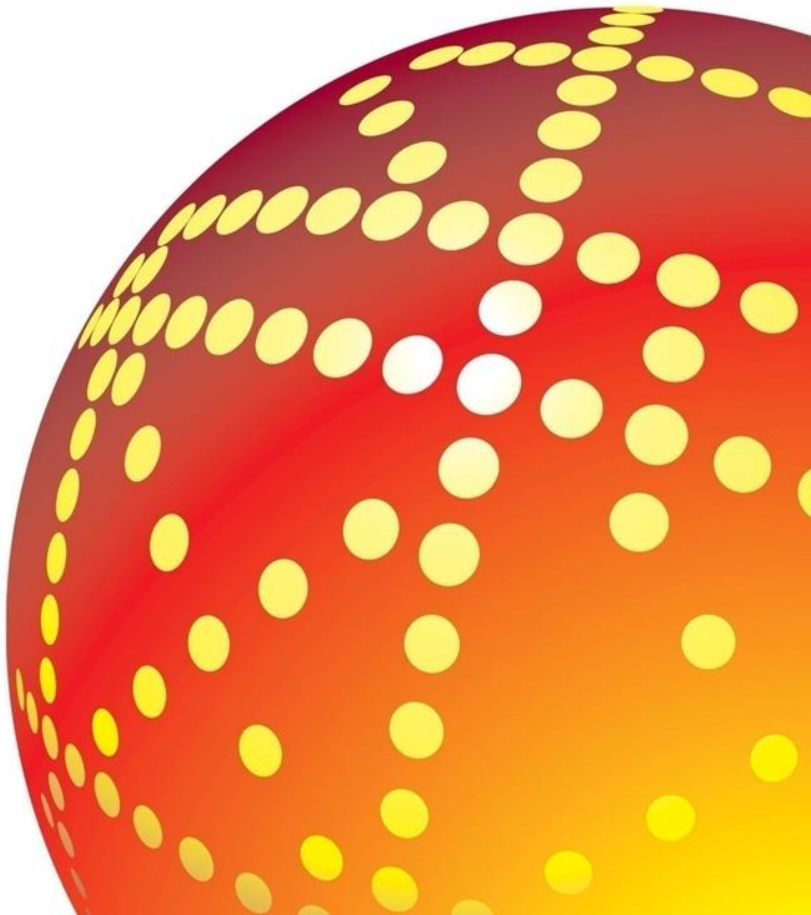
EUV Masks: Remaining challenges for HVM

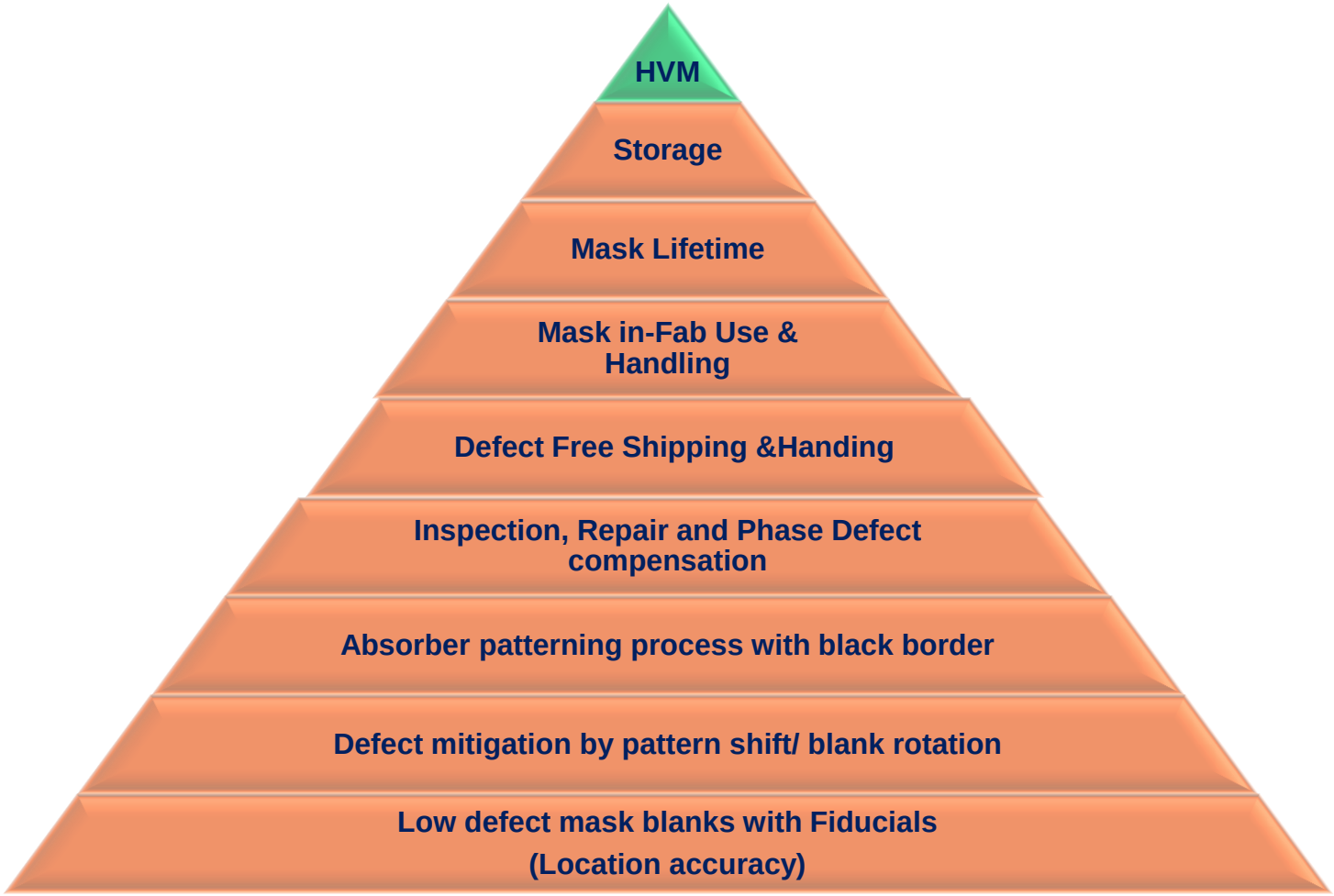
Pawitter Mangat



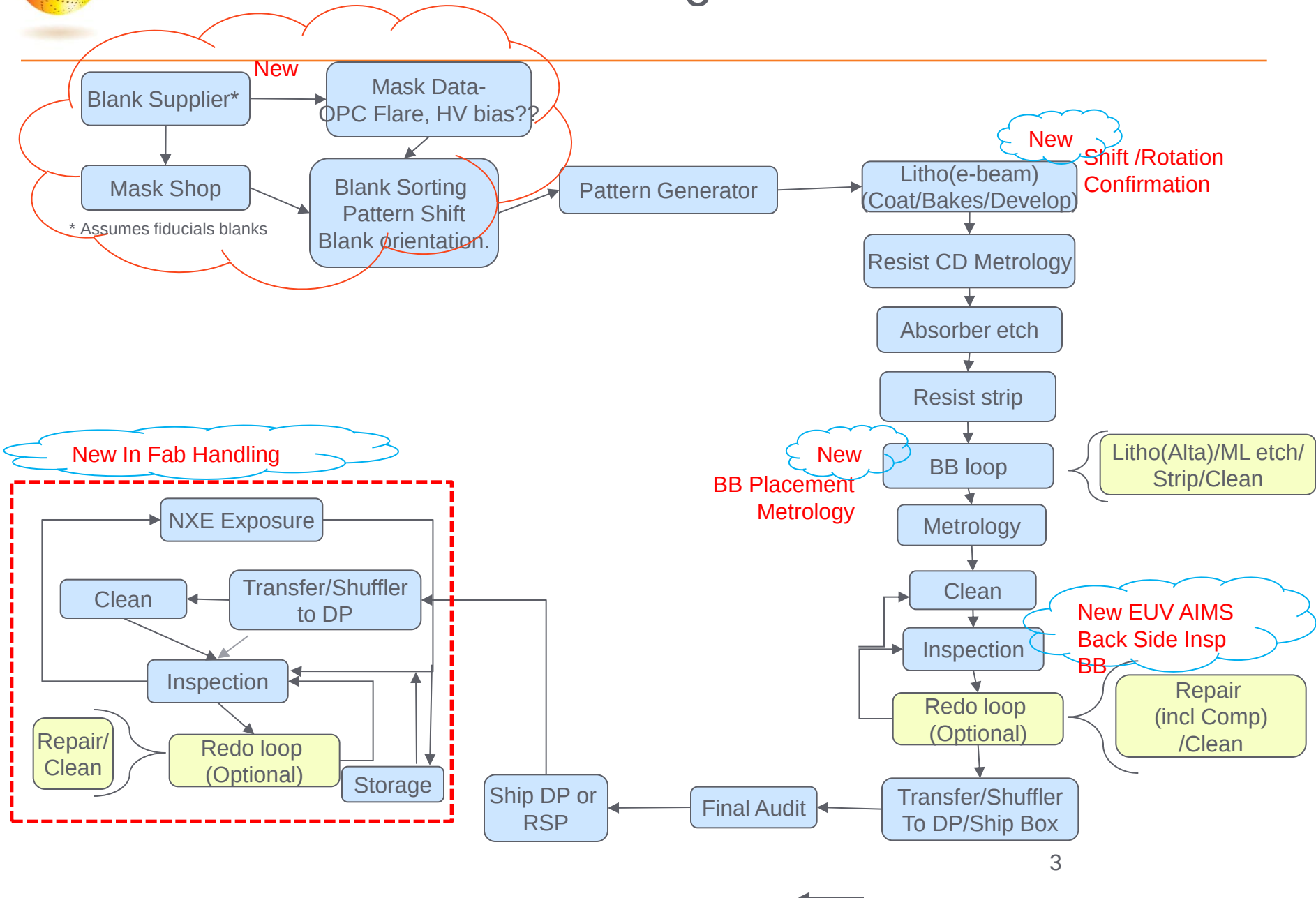
June 13, 2013

EUV Masks Challenge Pyramid

Zero defect printability needs a lot of Mask supporting infrastructure



EUV Mask Manufacturing flow-What is different?

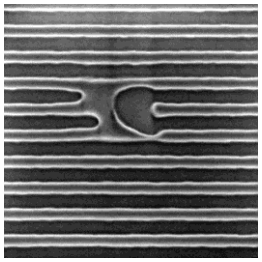


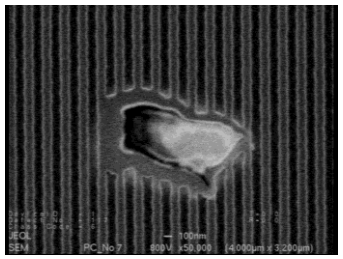
Mask Blank Gaps/Challenges

- Fiducial Strategy and Blank Supply with fiducials
  - SEMI P-48 task force
- Defect location accuracy relative to fidcuials
- Upfront Identification of blank defects that print
- Defects > 100nm
  - Difficult to hide/repair by defect mitigation approach
  - Primary cause is deposition process

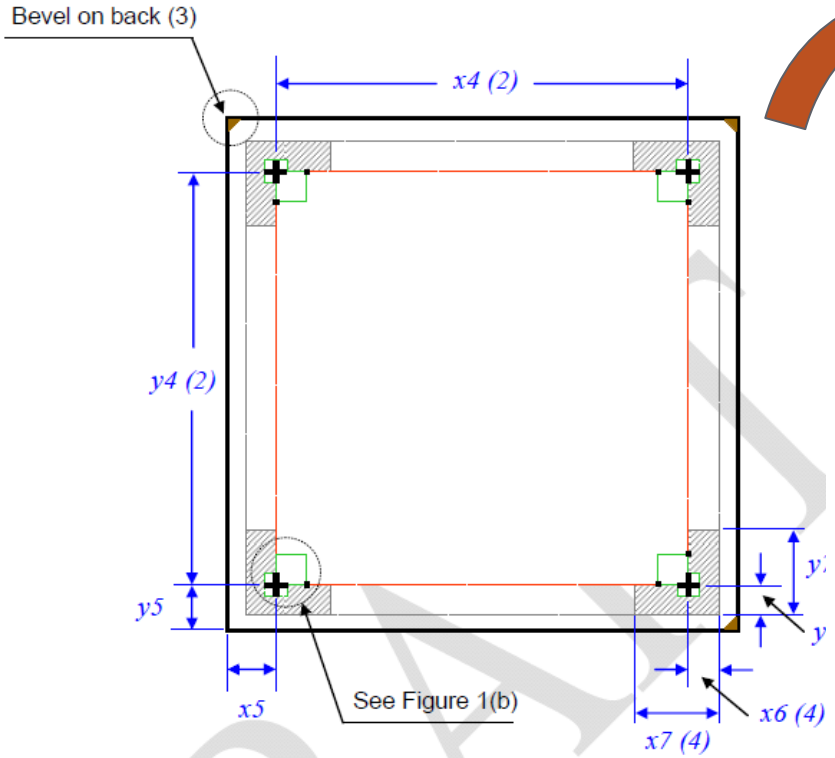
Gaps for Pattern-Shift

- Standardized FM set compatible with Blank defect inspection tools and ebeam writers
- Improved placement accuracy of FM to avoid need for pre-measurement of FM location
- Availability of defect maps relative to FM marks from Blank vendor
- Correction of Defect map to ebeam grid necessary via
  - (1) grid correlation Mask-shop vs. Blank-Vendor or
  - (2) pre-measured FM location provided by Blank Vendor (pre-measurement of FM location at Mask-shop less desirable)
- Setup of automated interface for registration of needed parameter to ebeam writer
- Functionality on ebeam writer to implement pattern-shift relative to FM w/o change of single chip placements (e.g. single shift parameter)





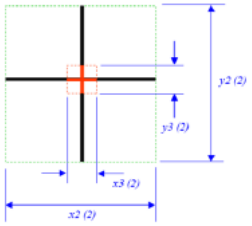
Fiducial SEMI P-48 draft under reconsideration



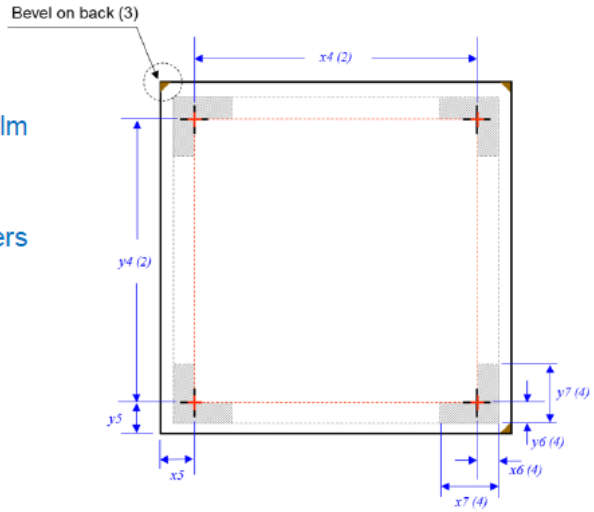
Revision And Status

Agreement reached for three (3) changes:

1. Define where vertically in the film stack to pattern markers
2. Remove all small crosses
3. Update current P48 placeholders with proven specifications



New Marker



New layout, with a partial marker at the unbeveled corner.

02/24/2013 2

Consensus Needed
URGENT!!!

Fiducial SEMI P-48 draft –Supplier prespective

SEMI P48 revision

AGC agrees with the current SEMI-P48 revision except for cross line depth.
AGC proposal is 50-200nm, instead of current depth specification (100-200nm).

Figure and table from SEMI P48 revision draft

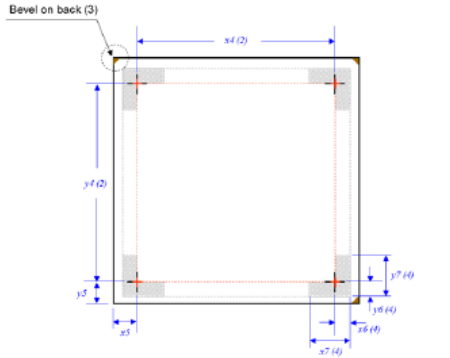


Figure 3 Fiducial Mark layout

Fiducial marks are placed on the frontside of mask blanks, one cross at each beveled corner and a partial cross at the un-beveled corner.

Table 1 Fiducial Mark Specification

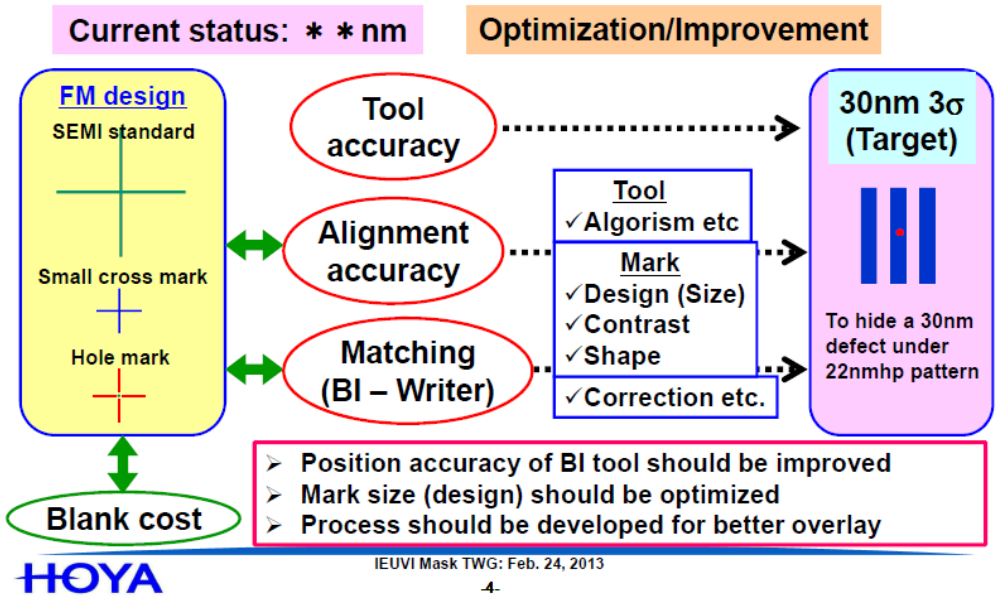
Symbol Used	Figure	Value (mm unless specified)	Tolerance (mm unless specified)	Reference Measured From	Feature Measured To
x2, y2	1, 2	0.550	±0.050	One line end of crosses	The other line end of the
x3, y3	1, 2	0.015 (TBD)	±0.001	Boundary of th of crosses as ind	
x4, y4	3	136.000	±0.010	Centers of cross	
x5, y5	3	8.000	±0.050	Centers of cross	
x6, y6	3	≤2.700		Centers of cross	
x7, y7	3	≤5.700		Outer lines of es	
FMPS Orthogonality		≤0.015/136.000 (≤110 µrad)		Any one side of	
FMPS Parallelism		≤0.200/136.000 (≤14.7 µrad)		Any one side of	
Cross line depth		100 – 200 nm (TBD)	TBD	Top of cross lin	
Cross line sidewall angle		TBD	TBD	Reference to the blanks	
Reflectivity differential		>13% (TBD)		Delta between r top and bottom	

50-200nm

"Look Beyond" AGC

Consensus Needed
URGENT!!!

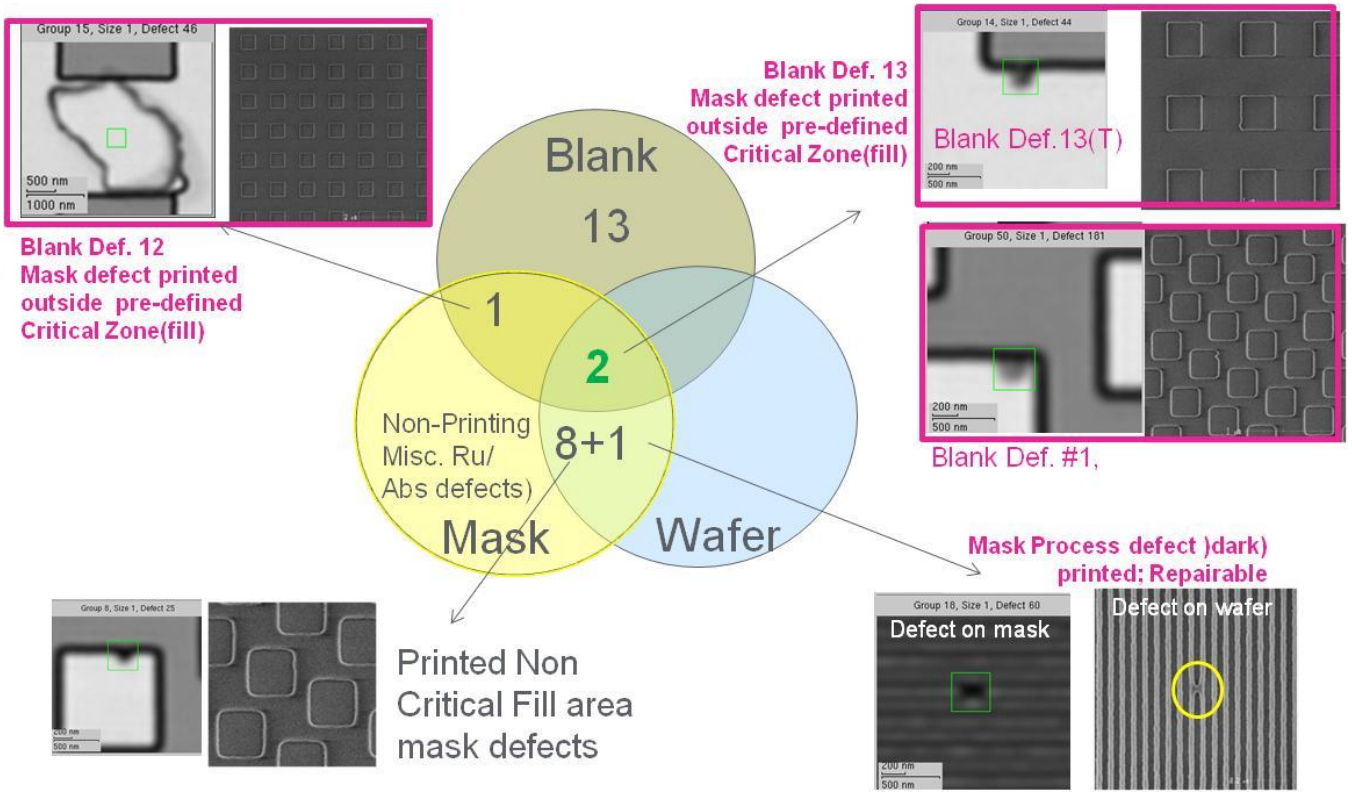
Needs more development toward 30nm accuracy



HOYA

20nm Integration Mask defect printability result

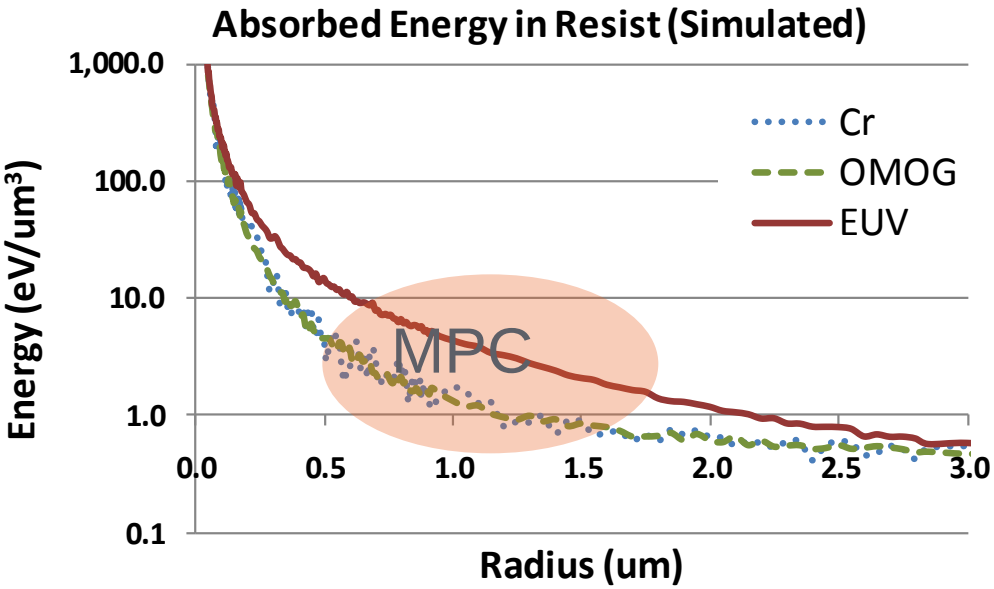
- Integration flows showing promising results for early confidence building but will not be sufficient For HVM
  - Blank Sorting vs layout
  - Blank orientation and pattern shift selection to hide blank defects under absorber (dark pattern) or fill region
  - Identify critical area for defect hiding on the layout
  - Printed without Repair; Only 1 repairable defect in critical area



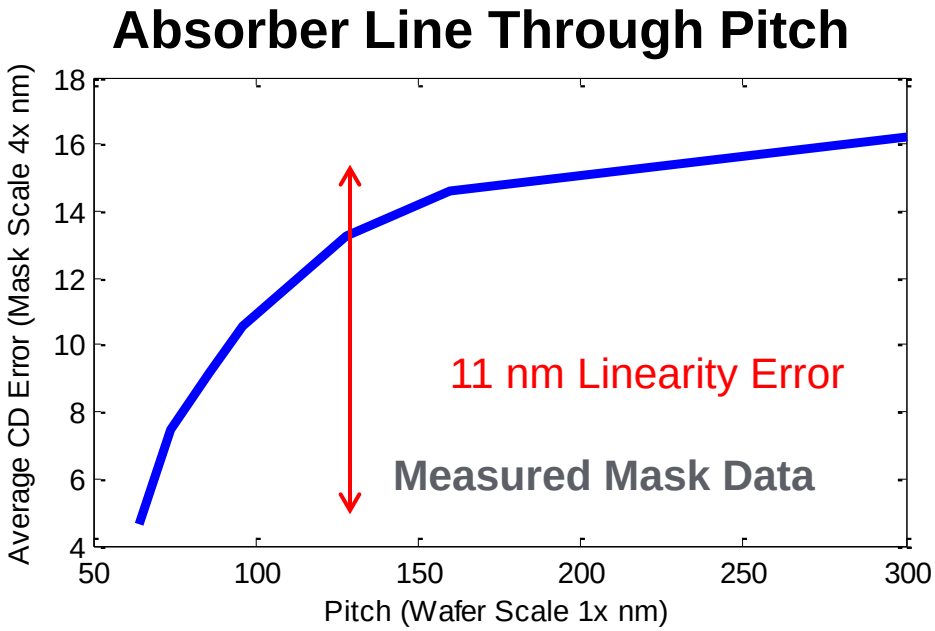
Mask Making-MPC

EUV Electron Backscatter

- Electron backscatter from EUV mask blank material large compared to DUV masks
- This causes short range variation in printing
  - Worst Case Example: Through pitch variation of absorber line
  - Variation MUCH larger than 0.3nm error allowance
- Not corrected by state of the art mask writers
- Not (explicitly) modeled in OPC

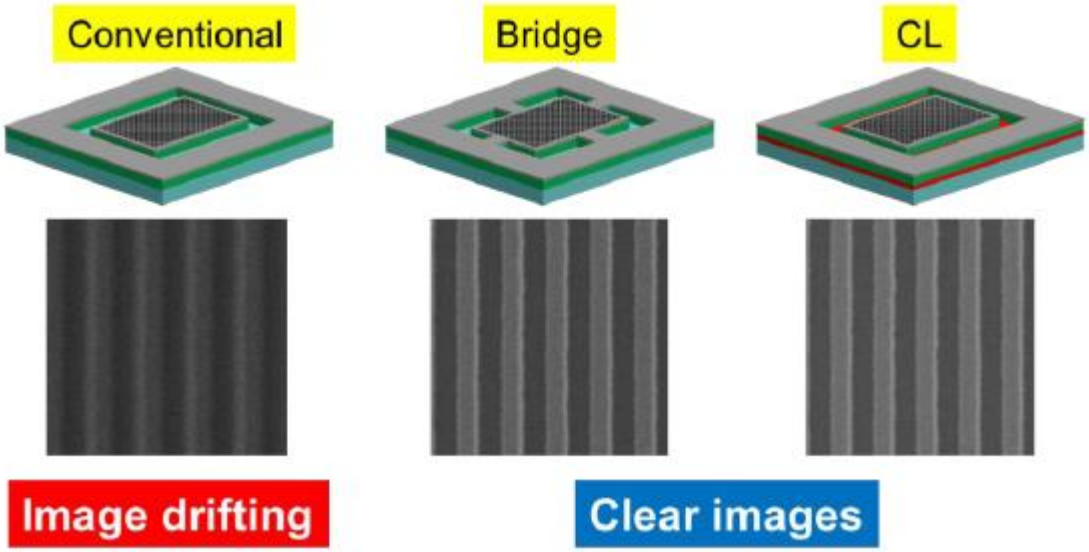


Monte Carlo Simulation Performed with PENELOPE

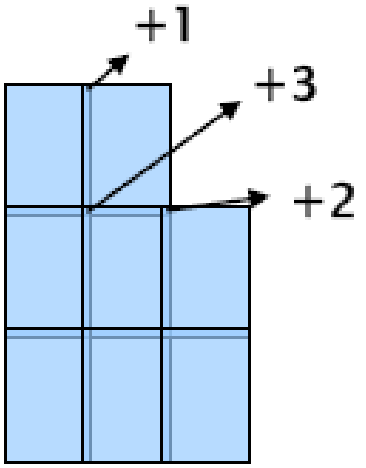


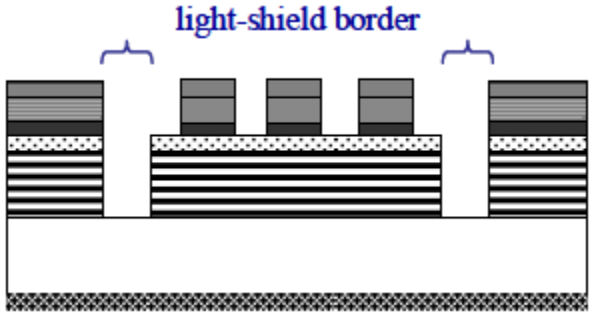
Black Border-Added Challenges

- Additional mask process steps - added Cycle time
- Impacts
  - Placement accuracy relative to die layout
  - Defect Inspection within BB area
  - Defect Inspection proximity to BB Area
  - Role of cleans for mask lifetime
  - Impact on CD Metrology (ESD/CD drift)



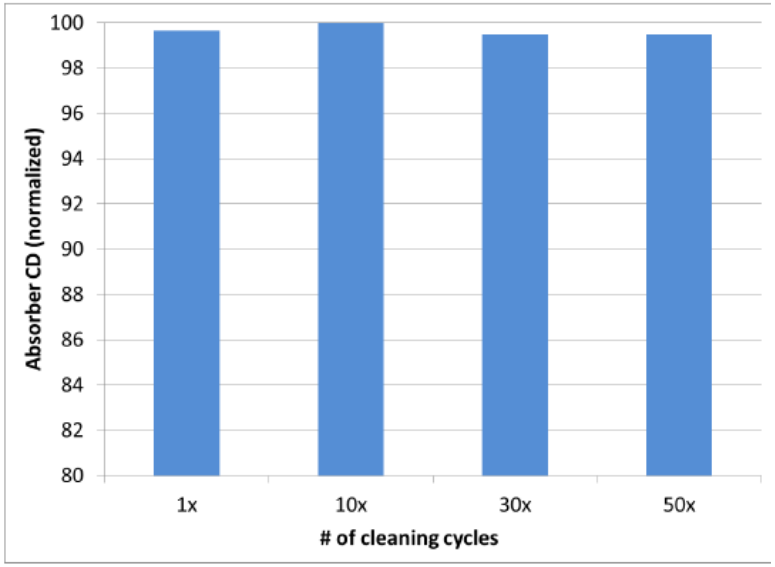
T. Katai et. al, PMJ 2013





Mask Cleans- Maximizing Lifetime is essential

50x Marathon Clean (Latest Data)

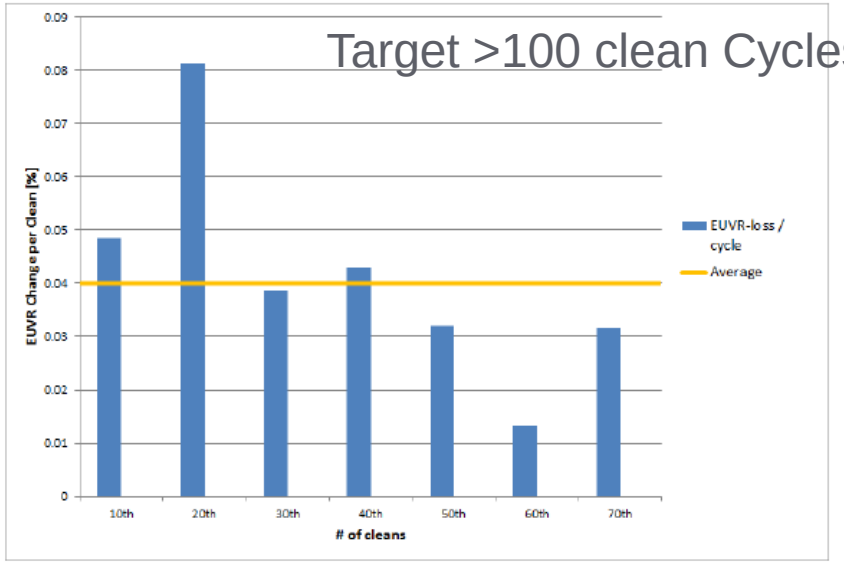


+ Mask CD shift at mask level is controlled within 0.15 Å per clean
+ No detectable impact on Mask CD Uniformity

22 | Remaining EUVL Mask Cleaning Challenges
IEUVI Mask TWG San Jose, CA February 24, 2013

70x Marathon Clean (Latest Data)

Target >100 clean Cycles



+ EUV Reflectivity is increasing throughout 70 cleaning cycles.
+ Average EUV Reflectivity increase is 0.04% per clean

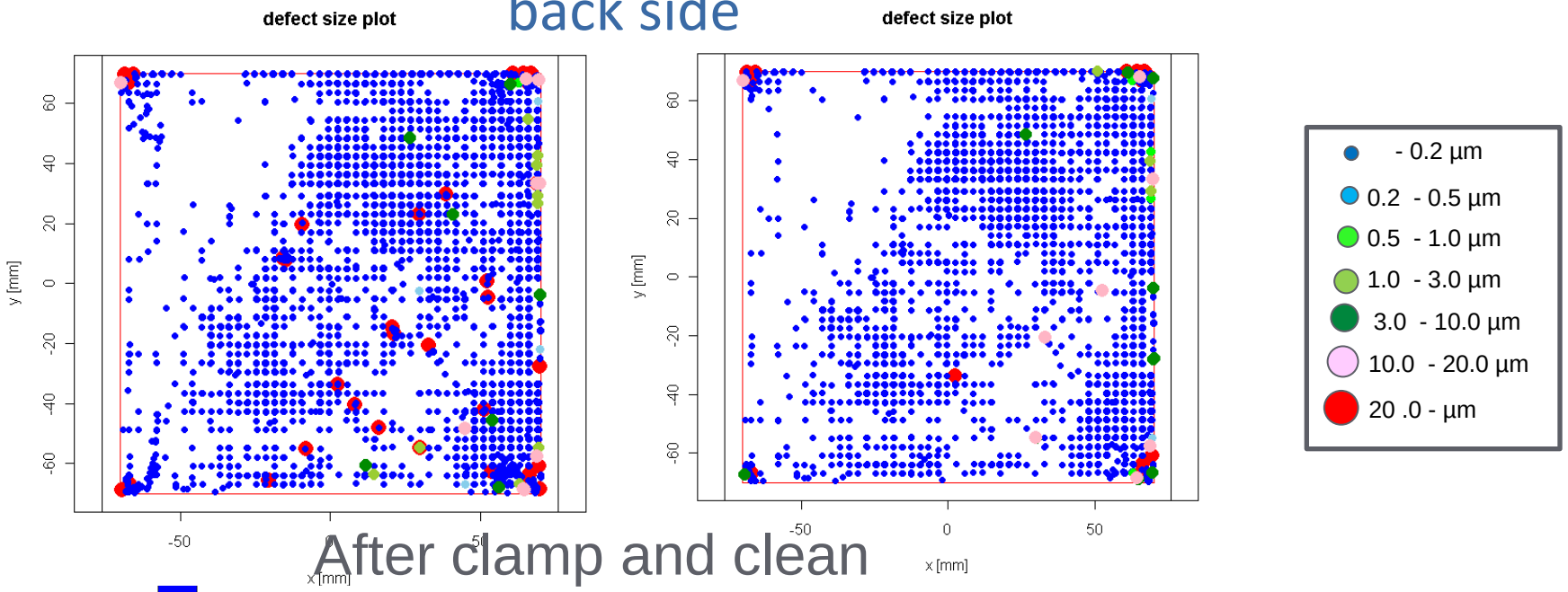
23 | Remaining EUVL Mask Cleaning Challenges
IEUVI Mask TWG San Jose, CA February 24, 2013

Suss Mircotec

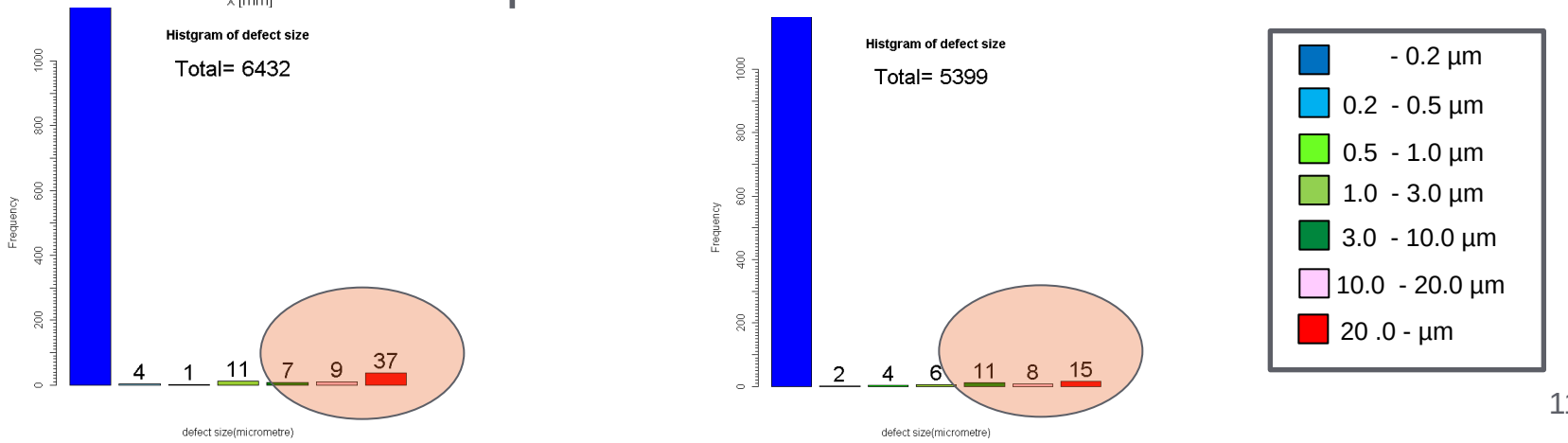
- Opportunity for Dry Cleans to maximize lifetime
  - Key Parameters: Ru Surface Roughness, Absorber Modification, Absorber CD control, EUV reflectivity, Front and Backside PRE

Added Mask Lifetime Challenge-Back Side Mask Defectivity after exposure

back side

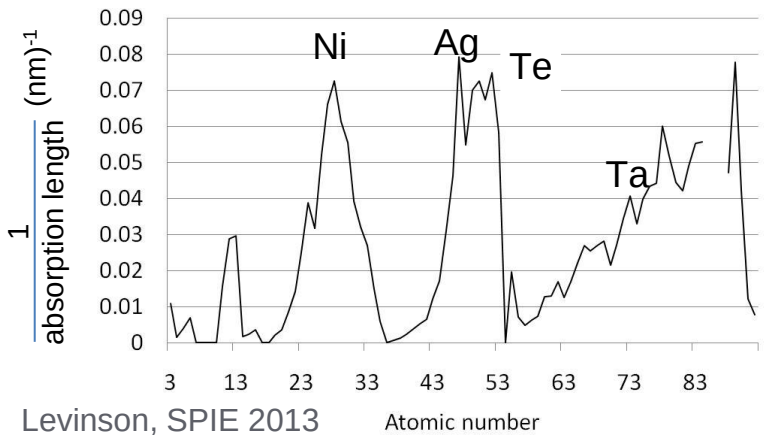


After clamp and clean



New Opportunities-EUV masks

- Thin absorber
  - Essential for EUV Extensibility
    - HV Bias, Telecentricity (PP)
  - Meet all current absorber requirements inc.
    - Plasma etching
    - Cleaning, Inspection, Repair
    - Durability under exposure.



Levinson, SPIE 2013

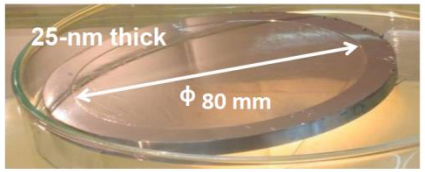
- Pellicle development
  - Significant progress shown
  - Need full integrated solution
    - Adhesive, Outgassing
    - Frame definition
    - Inspection strategy…

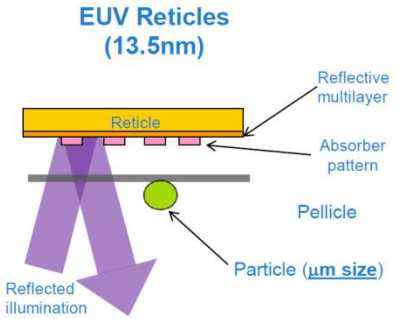
EUV pellicle considered as backup with minimum transmission and imaging loss

ASML

Public

Slide 26



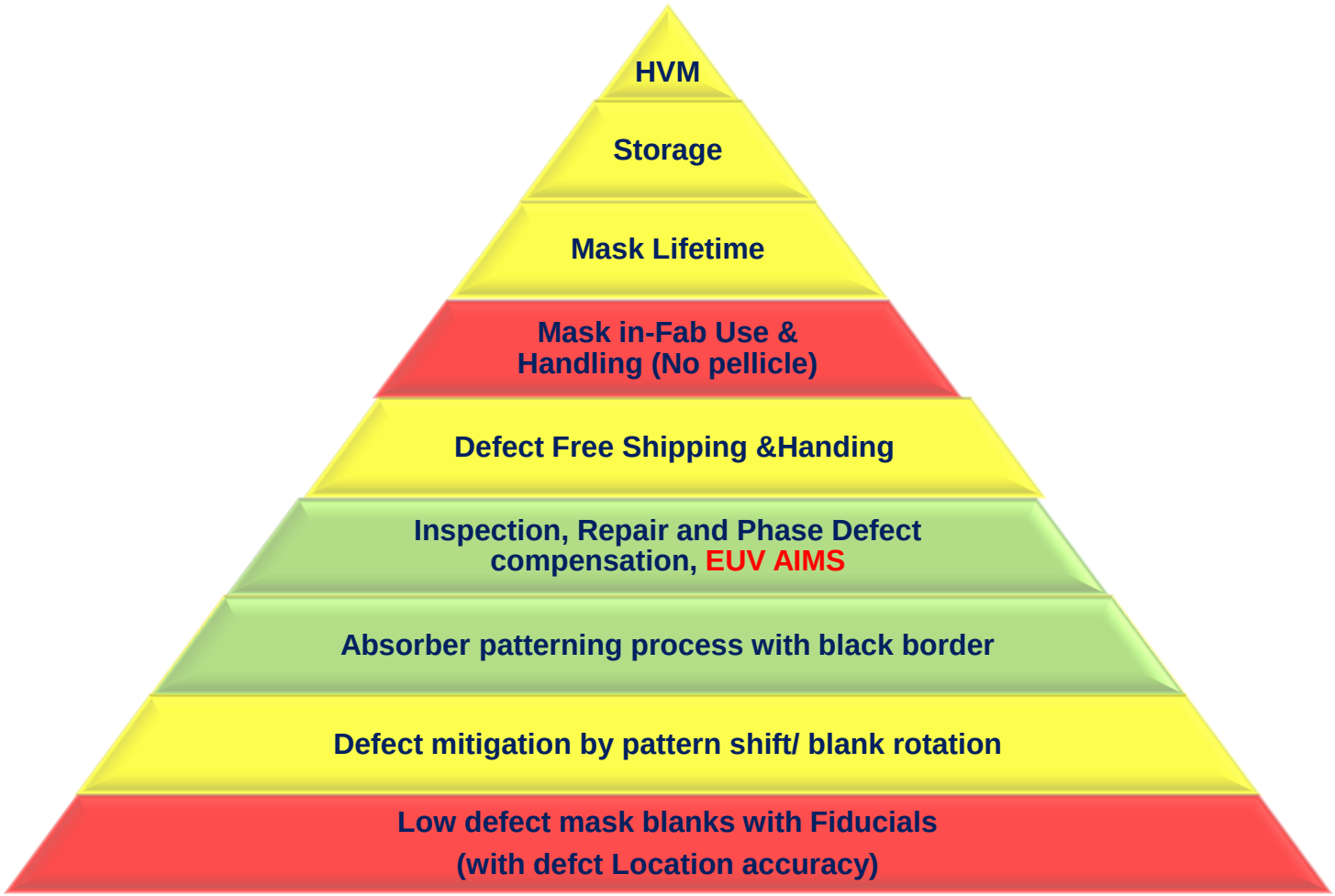


- Requirement: 90% transmission, 114x142 mm²
- Status: 87% transmission, ϕ 80 mm

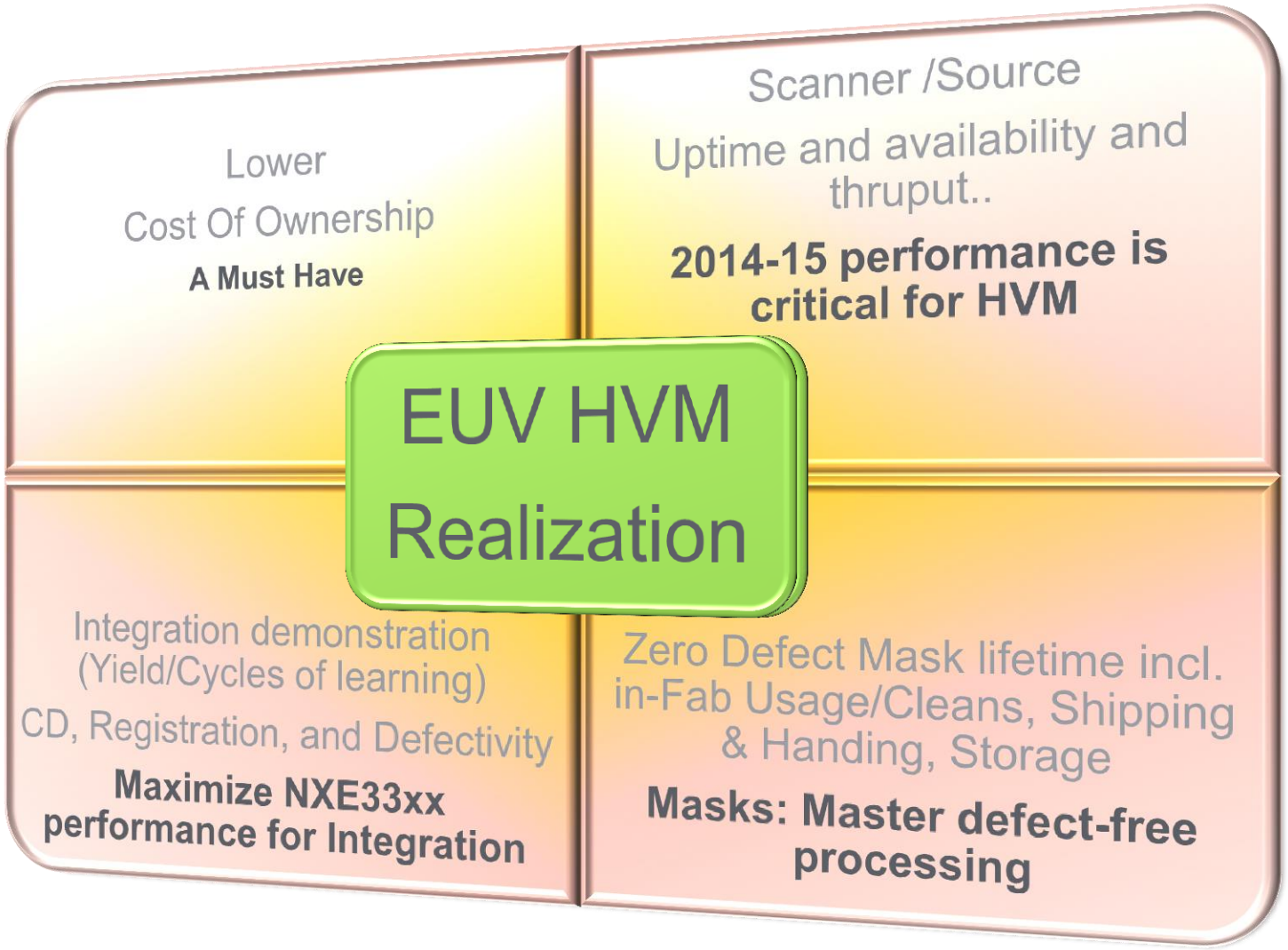
'resentation: Luigi Scaccabarozzi (ASML)

EUV Masks Challenge Summary

Zero defect printability needs a lot of Mask supporting infrastructure



Summary


Lower
Cost Of Ownership
A Must Have
Scanner /Source
Uptime and availability and thruput..
2014-15 performance is critical for HVM
EUV HVM Realization
Integration demonstration (Yield/Cycles of learning)
CD, Registration, and Defectivity
Maximize NXE33xx performance for Integration
Zero Defect Mask lifetime incl. in-Fab Usage/Cleans, Shipping & Handing, Storage
Masks: Master defect-free processing

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